PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. 13757US03)

In The Application Of:	
Amir Morad, *et al.*	
Serial No.: 10/776,541	
Filed: February 10, 2004	**Filed electronically on**
For: SYSTEM AND METHOD FOR VIDEO AND AUDIO ENCODING ON A SINGLE CHIP	**December 30, 2009**
Examiner: VO, TUNG T.	
Group Art Unit: 2621	
Confirmation No. : 3126	

PRE APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Applicants request review of the final rejection in the above-identified application (the "Application"). No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reasons stated on the attached sheets.

Respectfully submitted,

Date: December 30, 2009

By: /Kevin E. Borg/
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REMARKS

The Application includes pending claims 10-36, all of which have been rejected. Applicants respectfully submit that the claims define patentable subject matter.

Claims 10-20 and 24-33 were rejected under 35 USC §102(e) as being anticipated by Hinchley, *et al.* (US 6,490,250, hereinafter "Hinchley"). Claims 21-22 and 34-35 were rejected under 35 USC §103(a) as being unpatentable over Hinchley in view of Ishihara, *et al.* (US 6,516,031, hereinafter "Ishihara"). Claims 23 and 36 were rejected under 35 USC §103(a) as being unpatentable over Hinchley in view of Ishihara, and further in view of Kopet, *et al.* (US 5,448,310, hereinafter "Kopet").

Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 were rejected under 35 USC §103(a) as being unpatentable over Krishnamurthy, *et al.* (US 6,665,872, hereinafter "Krishnamurthy"). Claims 13 and 26 were rejected under 35 USC §103(a) as being unpatentable over Krishnamurthy in view of Bruck (US 6,519,289). Claims 14, 17-19, 27, and 30-32 were rejected under 35 USC §103(a) as being unpatentable over Krishnamurthy in view of Hinchley. Claims 21-22 and 34-35 were rejected under 35 USC §103(a) as being unpatentable over Krishnamurthy in view of Boice, *et al.* (US 6,823,013, hereinafter "Boice"). Claim 23 appears to have been rejected under 35 USC §103(a) as being unpatentable over Krishnamurthy in view of Boice, and further in view of Kopet. The Applicant respectfully traverses the rejections for at least the following reasons.

Regarding Applicants' independent claims 10 and 24, Applicants submit that Hinchley at least fails to disclose (1) "multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio," (2) "wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output

of the device," and "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device," (3) "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder," in accordance with Applicants' claims 10 and 24.

Regarding Applicant's independent claims 10 and 24, Applicants submit that Krishnamurthy at least fails to disclose (1) "multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio," (2) "wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device," and "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device," (3) "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder," in accordance with Applicants' claims 10 and 24.

With respect to Hinchley, the Office Action alleges that:

(a) Applicants' claimed "multiplexer circuitry" is disclosed in Applicants' Specification at Fig. 5, and that Hinchley's disclosure of MPEG-2 compliant "Mux Logic 750" having multiplexing operations of MPEG-2 has the same functions as Applicants' "multiplexing processor 114" of Fig. 5 and therefore anticipates the claimed features. (Office Action at page 2, line 14 - page 6, line 3); and

(b) Hinchley teaches a multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder. (Office action at page 6, lines 15-17).

With regard to Krishnamurthy, the Office Action alleges that:

(c) Krishnamurthy's "stat-mux board 308" teaches Applicants' multiplexer circuitry having first and second modes to produce first or first and second multiplexed streams

via first and second outputs, as claimed. (Office Action at page 7, line 12 to page 9, line 12);

(d) Krishnamurthy's "CPU 304" controls all elements of the "circuit board" of FIG. 3, and therefore would synchronize, coordinate, or harmonize all operations of the elements of FIG. 3, thus teaching Applicants' "control circuitry" synchronizing the first encoder, the second encoder, and the multiplexing circuitry, and that Krishnamurthy's teaching of an MPEG-2 encoder chip would obviously have a control function to synchronize the multiplexer, audio, and video encoders according to MPEG-2 standards. (Office Action at page 9, lines 13-22).

Applicants note that the Office has misinterpreted the teachings of Hinchley and Krishnamurthy for at least the following reasons.

First, with regard to (a), the Office argues anticipation by asserting that Applicants' FIG. 5 and paragraphs [0040], [0061], [0063], and [0064] are supporting disclosure for Applicants' claimed "multiplexing circuitry," that Hinchley's "Mux Logic 750" teaches Applicants' "mux 114" of FIG. 5, and therefore teaches Applicants' claimed "multiplexing circuitry." Initially, Applicants submit that the claims define the meets and bounds of the invention, not a portion of the disclosure selected by the Office, and that it is the claims that are to be examined against the prior art. Applicants submit that the Office is improperly limiting the scope of claims 10 and 24 to the teachings of the Application portions selected by the Office, and has not considered pages 5-9 of Applicants' Provisional Patent Application No. 60/296,766 incorporated by reference in the Application at the time of filing. Further, the Office implies that because Hinchley's "Mux Logic 750" is compliant with MPEG-2, that "Mux Logic 750" (inherently) performs Applicants' claimed multiplexing. The Office fails to identify support for this assertion. Further, Applicants' claims 10 and 24 require that the second mode concurrently produce a first multiplexed stream from first video and first audio, and produce a second multiplexed stream from the second video and the second audio. The Office fails to show support in Hinchley for output of two streams of multiplexed data. Instead, Hinchley states that a single stream is produced (Abstract), and Hinchley's "Mux Logic 750" shows only one output "224." Thus, because Hinchley does not teach first and

second modes and does not teach two streams of multiplexed output, the Office Action's assertion that Hinchley anticipates and therefore teaches all aspects of Applicants' claims 10 and 24, **amounts to clear error**.

Second, with regard to (b), the Office asserts that Hinchley's "multimedia engine 250" teaches "control circuitry" that "synchronizes the multiplexing circuitry, the first encoder, and the second encoder." Applicants have addressed this argument. *See* April 16, 2009 response at page 15-16. Hinchley merely teaches that the "multimedia engine 250" adjusts a "data rate" of only an encoder, but says nothing about "synchronization." Applicants submit that adjusting a "data rate" is quite different from "synchronization" Therefore, the Office Action's assertion that Hinchley's disclosure of a multimedia engine, which adjusts a data rate of an encoder, teaches synchronization of multiplexing circuitry, a first encoder, and a second encoder, **amounts to clear error**.

Third, with regard to (c), Applicants have shown that the "multichannel mode" allegedly taught by Krishnamurthy relates to "frame signals" used to transmit "statistical parameters," not to a "first mode" and a "second mode" of multiplexing combinations of "first compressed video," "first compressed audio," "second compressed video," and "second compressed audio," as claimed. *See* April 16, 2009 response at pages 21-24. Further, the Office asserts that Applicants' "first output" and "second output" coupling the "first multiplexed stream" and "second multiplexed stream" to external circuitry are taught by outputs of "stat mux 308" transmitted to elements "506, 510, and 330" of FIG 5. Applicants submit that FIG. 5 of Krishnamurthy illustrates details of "stat-mux 308." Therefore, cited elements "506, 510, and 330" of Fig. 5 are part of "stat-mux 308," and are therefore not external to the circuitry of "stat-mux 308," as required by claims 10 and 24. Further, the asserted teaching of "on-chip DMA" moving data from "TS output buffer" to a "serial port," at cited col. 19, lines 50-52 of Krishnamurthy, does not teach outputs of "stat-mux 308," asserted to teach Applicants' "multiplexer circuitry." Instead, the cited portion refers to serial transmission via "SSI" output of "encoder board 306," not "stat-mux 308." Further, "SSI" data is received by "stat-mux 308," not transmitted to external circuitry. Therefore, because Krishnamurthy's "multichannel mode" does not teach Applicants' "first mode" and "second mode", and the "SSI" outputs do not teach

Applicants' "first output" and "second output," the Office Action's allegation that Krishnamurthy teaches these claimed features, **amounts to clear error**.

Fourth, with regard to (d), Applicants have previously addressed this rejection. *See* April 16, 2009 response at pages 29-35. The Office Action alleges that Krishnamurthy's "CPU 304" teaches "synchroniz[ation], coordinat[ion], harmoniz[ation]." The Office offers only a conclusory statement, and does not explain how and where Krishnamurthy's teaches "CPU 304" performs synchronization of a "first encoder," "a second encoder," and "multiplexing circuitry," as claimed. Instead, the Office simply asserts that it would be "obvious" to modify "CPU 304" to perform the "synchronization." The "explicit analysis" required by MPEP §2142 is not provided. Applicants submit that "control" and "synchronization" are quite different. Therefore, because Krishnamurthy teaches "control" but not "synchronization," and the Office does not properly support its assertion of "obviousness," the Office Action's allegation that Krishnamurthy's "CPU 304" teaches "synchronizing," as claimed, **amounts to clear error**.

Therefore, because Hinchley and Krishnamurthy fail to teach or suggest all aspects of claims 10 and 24, the respective rejections under 35 USC §102(e) and 35 USC §103(a) cannot be maintained. Applicants also note that Bruck, Hinchley, Boice, and Kopet fail to remedy the deficiencies of Krishnamurthy. In addition, Applicants note that claims 11-23 and 25-36 depend, respectively, from independent claims 10 and 24, and are allowable for at least the reasons set forth above.

Thus, Applicants submit that claims 10-36 should be in condition for allowance and request that the outstanding rejections be reconsidered and withdrawn. The Commissioner is authorized to charge any necessary fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

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